REMARKS

Status of the Application

Claims 1-20 and 39-43 are pending in the application. Claims 39-43 have been withdrawn by the Examiner subject to a Restriction Requirement. Claims 1-20 have been Examined.

Applicant has added new claims 44-46. Applicant respectfully submits that the new claims are fully supported by the disclosure. No new matter has been added.

After entry of this Amendment, claims 1-20 and 39-46 will be pending in the application.

Restriction Requirement

The Examiner issued a Restriction Requirement and withdrew new claims 39-43 from consideration, alleging that claims 1-20 and claims 39-43 are related as subcombinations which are usable together in a single combination, but are distinct because they are also separately usable. Specifically, the Examiner states that claims 39-43 are directed to memory module ports/terminals which are distinct from the ring bus of claims 1-20.

As defined in MPEP § 806.05(a), a subcombination is an element of a combination. Claims 1-20 are directed to a memory system comprising, among other elements, memory modules, a controller, a bus and a CPU. Claims 41-43 are also directed to a memory system comprising, among other elements, memory modules, a controller, a bus and a CPU. Thus, claims 1-20 and 41-43 are directed to the same invention and are not related as subcombinations. Therefore, Applicant respectfully submits that the restriction of claims 41-43 is improper, and respectfully requests that the Examiner reconsider the restriction of claims 41-43.

Claim Rejections

Claims 1, 3 and 6 --- 35 U.S.C. § 103(a)

Claims 1, 3 and 6 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,658,509 to Bonella *et al.* ("Bonella") in view of U.S. Pat. Pub. No. 2002/0078280 to Arimilli *et al.* ("Arimilli") and U.S. Pat. Pub. No. 2002/0069317 to Chow *et al.* ("Chow"). Applicant traverses this rejection.

Claims 1, 3 and 6 are patentable over the combination of Bonella, Arimilli and Chow for at least the reasons set forth below because, absent impermissible hindsight based on Applicant's disclosure, one of ordinary skill in the art at the time the invention was made would not have been motivated to combine the references as attempted by the Examiner.

As claimed by Applicant, a control device switches an operational mode of a ring bus from a unidirectional bus which either sends or receives a signal unidirectionally, to a bi-directional bus which sends and receives a signal bi-directionally, when an arbitrary memory module is being removed. When an arbitrary memory module is missing from the ring bus, data which would have been written to or read from the missing memory locations is instead written to or read from a hard disk device. Thus, by providing a hard disk device for interim data storage and the dual unidirectional and bi-directional operational modes of the ring bus, Applicant's invention provides continued ability to read from and write to data storage locations even in the absence of an arbitrary memory module. The combined references do not address this problem or suggest the claimed combinations.

The primary reference, Bonella, is directed to a ring bus architecture in which half of each data word is sent in opposite directions around the ring bus, passing through buffers on memory modules in the path, to be recombined at a buffer of a destination memory module.

Thus, when data is written to a memory module, each half of the data word will be transmitted in opposite directions around the ring bus through the memory module buffers which are in the path between the controller and the destination memory module. The read operation is similarly performed by sending half of each data word in opposite directions around the ring bus from the memory module from which it was read to the controller, where the half data words are recombined to form a full data word.

By sending half of each data word in opposite directions around the bidirectional loop, Bonella discloses the advantage of using only half as many bus lines. See column 3, lines 45-67. Thus, each portion of Bonella's ring bus must always operate in a bidirectional mode to perform read/write operations with a target memory module.

As illustrated in figures 13 and 14 of Bonella, each memory module includes memory devices as well as data redrive/transfer logic (i.e., buffers). Since each half of the data word is sent in opposite directions around the ring bus, removing a module would remove from the ring bus architecture the buffers necessary to transmit a half data word in one of the required directions around the ring bus. A missing module would result in loss of half of each data word at the target memory module since the ring bus architecture of Bonella operates only in a bidirectional mode. Bonella does not contemplate ring bus operation in a unidirectional mode.

Thus, Bonella does not even recognize the problem solved by Applicant's invention, since the invention does not compensate for the missing memory module and maintain the ability to seamlessly read and write data. Further, the Examiner admits that Bonella does not disclose operating the bus lines in both a bidirectional and unidirectional mode, as required by the claim. Rather, the Examiner relies on Arimilli for teaching this feature.

The Examiner relies on Arimilli to allegedly disclose a control device which switches an operational mode of a ring bus from unidirectional to bidirectional. Arimilli discloses circuit modules, each of which has a transmitter/receiver that is selectable between a unidirectional mode and a bidirectional mode. However, the reference does not disclose much detail about the conditions under which the circuit modules would be switched from one mode to the other.

Arimilli merely discloses that the mode selection can be based on detecting environmental characteristics of the transmission lines. See paragraph [0019]. To the extent that the reference discloses continued system operation in the absence of an arbitrary module, Arimilli merely provides one example of a "hot-pluggable processor" as a circuit module. See paragraph [0014]. Therefore, Arimilli does not contemplate a solution to the problem of providing continued ability to read from and write to data storage locations in the absence of an arbitrary memory module.

Chow does not cure the above-noted deficiencies of the Bonella-Arimilli combination. The Examiner relies on Chow to allegedly disclose a hard disk drive to which data stored in the memory modules is copied at predetermined time periods. However, Chow's system is not intended for use in a ring bus memory system. In fact, Chow teaches away from its use in a ring bus memory system. In paragraph [0166], Chow states that an aspect of the invention is to use multiple links to couple the management module 125 to memory matrix modules 105 to form a "mesh" or "fabric type redundancy" that provides for a higher data transfer rate during normal operations. See paragraph [0166]. Thus, Chow teaches away from the use of a ring bus to connect the control device to the memory modules in combination with Bonella and Arimilli.

Thus, one of ordinary skill in the art merely having knowledge of the Bonella, Arimilli and Chow references would not have been motivated to combine the references as attempted by

the Examiner since, absent impermissible hindsight provided by Applicant's disclosure, the references do not suggest the combination of features as claimed by Applicant.

Accordingly, claim 1 is patentable over the combination of Bonella, Arimilli and Chow. Claims 3 and 6 are patentable at least by virtue of their dependence.

Claims 2, 4, 5, 7, 8 and 15-20 --- 35 U.S.C. § 103(a)

Claims 2, 4, 5, 7, 8 and 15-20 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella in view of Arimilli, Chow and U.S. Patent No. 5,586,291 to Lasker *et al.* ("Lasker"). Applicant traverses this rejection.

Claims 2, 4, 5, 7, 8 and 15-20 are patentable over the combination of Bonella, Arimilli, Chow and Lasker for at least the reasons set forth below.

Independent claims 2 and 5 contain features similar to the features recited in claim 1 and are therefore patentable over the combination of Bonella, Arimilli and Chow for reasons similar to the reasons established above for claim 1. Lasker is directed to a disk storage and cache memory system which allows faster data access by using volatile memory rather than disk storage for working data access (Abstract). Neither the portions of Lasker cited by the Examiner, nor any other portion of Lasker, discloses or suggests the above-noted features missing in the improper combination of Bonella, Arimilli and Chow.

Accordingly, claims 2 and 5 are patentable over the combination of Bonella, Arimilli, Chow and Lasker. Claims 4, 7, 8 and 15-20 are patentable at least by virtue of their dependence.

Claim 9 --- 35 U.S.C. § 103(a)

Claim 9 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella, Arimilli and Chow, and further in view of U.S. Patent No. 6,487,623 to Emerson *et al.* ("Emerson"). Applicant traverses this rejection.

Claim 9 depends from and incorporates the features of claim 1. As established above, claim 1 is patentable over the improper combination of Bonella, Arimilli and Chow. The Examiner relies on Emerson only to allegedly disclose an FET switch as a short-circuit device for short-circuiting or opening bus connections which are disconnected by removing a memory module. Emerson, however, discloses FET isolation buffers 160 which provide isolation of a RAM module 106 from a memory bus 105a for removal of the RAM module 106 (column 7, lines 12-25). Thus, Emerson does not cure the deficiencies of the Bonella-Arimilli-Chow combination.

One of ordinary skill in the art at the time the invention was made would not have been motivated to combine the references as attempted by the Examiner since the combined references do not disclose or suggest all of the claimed features. Accordingly, claim 9 is patentable over the combination of Bonella, Arimilli, Chow and Emerson.

Further, Emerson merely discloses the use of FET isolation buffers to isolate a connector containing a memory module for removal (column 8, line 50-, line 45). In fact, Emerson is ***directed to a parallel bus structure*** as illustrated in Fig. 1 of Applicant's specification rather than the recited ring bus structure and thus is ***silent as to providing a short-circuit or an open circuit in the bus structure as recited in the claims***.

Claim 9 is patentable for at least these additional reasons.

Claims 10 and 11 --- 35 U.S.C. § 103(a)

Claims 10 and 11 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella, Arimilli, Chow and Lasker, and further in view of Emerson. Applicant traverses this rejection.

Claims 10 and 11 are patentable over the combination of Bonella, Arimilli, Chow, Lasker and Emerson. Claims 10 and 11 depend from and incorporate the features of claims 2 and 5, respectively, which, as established above, are patentable over the improper combination of Bonella, Arimilli, Chow and Lasker. As also noted above in the arguments for claim 9, Emerson does not cure the deficiencies of the combined references.

One of ordinary skill in the art at the time the invention was made would not have been motivated to combine the references as attempted by the Examiner since the combined references do not disclose or suggest all the claimed features.

Accordingly, claims 10 and 11 are patentable over the combination of Bonella, Arimilli , Chow, Lasker and Emerson.

Claim 12 --- 35 U.S.C. § 103(a)

Claim 12 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella, Arimilli and Chow, and further in view of U.S. Patent No. 6,889,304 to Perego *et al.* ("Perego"). Applicant traverses this rejection.

Claim 12 is patentable over the combination of Bonella, Arimilli, Chow and Perego. Claim 12 depends from and incorporates the features of claim 1. As established above, claim 1 is patentable over the improper combination of Bonella, Arimilli and Chow. The Examiner relies on Perego to allegedly disclose a connector as a short-circuit device.

However, even if Perego provides such disclosure, the reference fails to cure the deficiencies of the improper combination of Bonella, Arimilli and Chow. Accordingly, claim 12 is patentable over the combination of Bonella, Arimilli, Chow and Perego.

Claims 13 and 14 --- 35 U.S.C. § 103(a)

Claims 13 and 14 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella, Arimilli, Chow and Lasker, and further in view of Perego. Applicant traverses this rejection.

Claims 13 and 14 are patentable over the combination of Bonella, Arimilli, Chow, Lasker, and Perego. Claims 13 and 14 depend from and incorporate the features of claims 2 and 5, respectively, which, as established above, are patentable over the improper combination of Bonella, Arimilli, Chow and Lasker. As also noted above in the arguments for claim 12, Perego does not cure the deficiencies of the combined references.

One of ordinary skill in the art at the time the invention was made would not have been motivated to combine the references as attempted by the Examiner since the combined references do not disclose or suggest all of the claimed features.

Accordingly, claims 10 and 11 are patentable over the combination of Bonella, Arimilli, Chow, Lasker and Perego.

New Claims

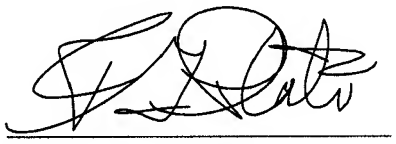
Applicant has added new claims 44-46. New claims 44-46 depend from claims 1, 2 and 5, respectively, and are patentable at least by virtue of their dependence.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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